L Number	Hits	Search Text	DB	Time stamp
1	6862	((717/151-155) or (716/1,3-5,7,11,13,18) or (703/2,14,21,23)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/07 13:33
3	5	(((717/151-155) or (716/1,3-5,7,11,13,18) or (703/2,14,21,23)).CCLS.) and netlist and HDL and synthesis and speculation and pipelin$4 and block and (sharing or shared) and (expression same function)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/07 13:36
-	592	(@ad<=20000807 or @rlad<=20000807) and (emulation or cosimulat$4 or co-simulat$4) and ((hardware and software) same (lay$4 or set$4 or configur$4 or mapp$4)) and compiler	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:01
-	2025	(HDL or Verilog or "hardware description language") and (pipelin$4 or schedul$4 or speculativ$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 11:59
-	50	HDL same pipelin$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 12:59
-	7	(HDL same pipelin$4) and (@ad<=20000807 or @rlad<=20000807) and (emulation or cosimulat$4 or co-simulat$4) and (hardware same software) and compiler	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 13:00
-	3	(HDL same pipelin$4) and (@ad<=20000807 or @rlad<=20000807) and runtime and (hardware same software) and compiler	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 13:00
-	14	(HDL same pipelin$4) and (@ad<=20000807 or @rlad<=20000807) and (hardware same software) and compiler	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 13:00
-	67	((@ad<=20000807 or @rlad<=20000807) and (emulation or cosimulat$4 or co-simulat$4) and ((hardware and software) same (lay$4 or set$4 or configur$4 or mapp$4)) and compiler) and ((HDL or Verilog or "hardware description language") and (pipelin$4 or schedul$4 or speculativ$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 13:01
-	6	(((@ad<=20000807 or @rlad<=20000807) and (emulation or cosimulat$4 or co-simulat$4) and ((hardware and software) same (lay$4 or set$4 or configur$4 or mapp$4)) and compiler) and ((HDL or Verilog or "hardware description language") and (pipelin$4 or schedul$4 or speculativ$4))) and (HDL same pipelin$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:03
-	127	(mapp$4 or translat$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 14:04
-	2025	(HDL or Verilog or "hardware description language") and (pipelin$4 or schedul$4 or speculativ$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 14:05

-	18	((mapp$4 or translat$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware)) and ((HDL or Verilog or "hardware description language") and (pipelin$4 or schedul$4 or speculativ$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 14:05
-	7	(((mapp$4 or translat$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware)) and ((HDL or Verilog or "hardware description language") and (pipelin$4 or schedul$4 or speculativ$4))) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 15:42
-	40	((flow or expression or pointer and array) same (hardware adj2 (circuit$5 or resource or entity or line or gate))) and compil$4 and (RTL or synthesis or (hardware adj2 definition))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 14:57
-	27	(((flow or expression or pointer and array) same (hardware adj2 (circuit$5 or resource or entity or line or gate))) and compil$4 and (RTL or synthesis or (hardware adj2 definition))) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:50
-	6	5650948.URPN.	USPAT	2004/08/05 15:15
-	6	5650948.URPN.	USPAT	2004/08/05 15:15
-	3	(speculat$4 and (block neare3 shar$4) and (loop near3 pipeline) and compiler and ((synthesis same hardware) or (HDL or Verilog or PLA or FPGA or cosimulation))) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 15:46
-	4	speculat$4 and (block neare3 shar$4) and (loop near3 pipeline) and compiler and ((synthesis same hardware) or (HDL or Verilog or PLA or FPGA or cosimulation))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 15:45
-	5	speculat$4 and (block neare3 shar$4) and (loop near3 pipeline) and compiler and ((synthesis or HLS) or (HDL or Verilog or PLA or FPGA or cosimulation or SystemC))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:27
-	2	(speculat$4 and (block neare3 shar$4) and (loop near3 pipeline) and compiler and ((synthesis or HLS) or (HDL or Verilog or PLA or FPGA or cosimulation or SystemC))) not ((speculat$4 and (block neare3 shar$4) and (loop near3 pipeline) and compiler and ((synthesis same hardware) or (HDL or Verilog or PLA or FPGA or cosimulation))) and (@ad<=20000807 or @rlad<=20000807))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 15:46
-	1	speculat$4 and (block neare3 shar$4) and (loop near3 pipeline) and ((HDL or Verilog or "hardware description language") and (pipelin$4 or schedul$4 or speculativ$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:05
-	1	(("flow graph" or (loop adj2 schedul$5)) same "high-level programming") and (optimi$5 and (hardware same (synthesis or netlist)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:08
-	8	((((flow or expression or pointer and array) same (hardware adj2 (circuit$5 or resource or entity or line or gate))) and compil$4 and (RTL or synthesis or (hardware adj2 definition))) and (@ad<=20000807 or @rlad<=20000807)) and ("high-level programming") and (optimi$5 and (hardware same (synthesis or netlist)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:17

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-	2	6219628.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 15:59
-	12	("5309556" | "5497498" | "5535342" | "5541849" | "5583749" | "5603043" | "5638299" | "5652875" | "5684980" | "5732277" | "5737235" | "6064409").PN.	USPAT	2004/08/05 16:00
-	74	5541849.URPN.	USPAT	2004/08/05 16:04
-	74	5541849.URPN.	USPAT	2004/08/05 16:04
-	70	((speculat$4 and (loop near3 pipeline)) or (block neare3 shar$4)) and ((speculat$4 or (block neare3 shar$4) or (loop near3 pipeline)) and 5541849.URPN.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:48
-	10	((speculat$4 or (modulo or pipeline))) and (((speculat$4 and (loop near3 pipeline)) or (block neare3 shar$4)) and ((speculat$4 or (block neare3 shar$4) or (loop near3 pipeline)) and 5541849.URPN.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:35
-	8	(pipeline and (block neare3 shar$4)) and ((speculat$4 or (block neare3 shar$4) or (loop near3 pipeline)) and 5541849.URPN.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:10
-	8	(((speculat$4 or (modulo or pipeline))) and (((speculat$4 and (loop near3 pipeline)) or (block neare3 shar$4)) and ((speculat$4 or (block neare3 shar$4) or (loop near3 pipeline)) and 5541849.URPN.))) and ((pipeline and (block neare3 shar$4)) and ((speculat$4 or (block neare3 shar$4) or (loop near3 pipeline)) and 5541849.URPN.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:10
-	23	(block near3 sharing) and (((mapp$4 or translat$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware)) or ((HDL or Verilog or "hardware description language") and (pipelin$4 or schedul$4 or speculativ$4)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:35
-	18	((block near3 sharing) and (((mapp$4 or translat$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware)) or ((HDL or Verilog or "hardware description language") and (pipelin$4 or schedul$4 or speculativ$4)))) and (hardware same (synthesis or netlist))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:18
-	23	(speculat$4 or (block neare3 sharing) or (loop near3 pipeline)) and compiler and ((((flow or expression or pointer and array) same (hardware adj2 (circuit$5 or resource or entity or line or gate))) and compil$4 and (RTL or synthesis or (hardware adj2 definition))) and (@ad<=20000807 or @rlad<=20000807))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:26
-	23	((speculat$4 or (block neare3 sharing) or (loop near3 pipeline)) and compiler and ((((flow or expression or pointer and array) same (hardware adj2 (circuit$5 or resource or entity or line or gate))) and compil$4 and (RTL or synthesis or (hardware adj2 definition))) and (@ad<=20000807 or @rlad<=20000807))) and ((synthesis or HLS or netlist) or (HDL or Verilog or PLA or FPGA or cosimulation or SystemC))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:27

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-	11	((speculat$4 or (modulo or pipeline))) and 5541849.URPN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:41
-	12	5751596.URPN.	USPAT	2004/08/05 16:41
-	8	(((speculat$4 or (modulo or pipeline) or (block near2 sharing))) and (netlist and synthesis)) and ("high-level programming") and ((optimi$5 or mapping) (hardware same (software or programming or RTL)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:43
-	26	((speculat$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 11:04
-	22	(((speculat$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:51
-	13	((((speculat$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler) and (@ad<=20000807 or @rlad<=20000807)) and (717/$ or 716/$ or 703/$ or 711/$ or 710/$)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:52
-	4	((speculat$4 and (loop near3 pipeline)) or (block near sharing)) and ((((speculat$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler) and (@ad<=20000807 or @rlad<=20000807)) and (717/$ or 716/$ or 703/$ or 711/$ or 710/$))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:58
-	5	(block near sharing) and ((((speculat$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler) and (@ad<=20000807 or @rlad<=20000807))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/05 16:58
-	216505	(VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:00
-	5412	optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:02
-	4915	(optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:02
-	1	((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and ((loop near2 pipelin$4) and (block near3 sharing))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:03
-	20	((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:21

-	12	((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:05
-	10	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:05
-	595	((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:04
-	487	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:11
-	10	((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:05

-	10	((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and ((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:05
-	764	((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:10
-	44	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:10
-	26	((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:24
-	26	(((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807)) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:19

-	26	(((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807)) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) not (((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and ((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and (((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:20
-	10	((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807)) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) not (((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and ((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing))))) and Gupta.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:20

-	12	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (speculat$5 and (block near3 sharing))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:22
-	0	((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (speculat$5 and (block near3 sharing))) and (VHDL or HDL or Verilog)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:32
-	1	((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (speculat$5 and (block near3 sharing))) and (netlist or ((hardware or circuit$4) near6 synthesis))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:23
-	635	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (speculat$5 or (block near3 shared))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:25
-	2040	(netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:29
-	1202	((netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:26
-	15	((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (speculat$5 or (block near3 shared))) and (((netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:26
-	15	(((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (speculat$5 or (block near3 shared))) and (((netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807))) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:30

-	5	(((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (speculat$5 or (block near3 shared))) and (((netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807))) and (@ad<=20000807 or @rlad<=20000807)) not (((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807)) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) not ((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and ((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (@ad<=20000807 or @rlad<=20000807)) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing))))))) and Gupta.in.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:27
-	73	(netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:30
-	35	((netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))) and (@ad<=20000807 or @rlad<=20000807)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:30

-	1	(netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared)) and ((US-6505339-$ or US-6226776-$ or US-6026219-$ or US-5764951-$ or US-6625797-$ or US-6608638-$ or US-6415420-$ or US-6519742-$ or US-6035123-$ or US-5819064-$ or US-5706205-$ or US-5696956-$ or US-5650948-$ or US-6389587-$ or US-6360355-$ or US-6219628-$ or US-5652875-$ or US-5541849-$ or US-6588004-$ or US-6505340-$ or US-6080204-$ or US-5870308-$ or US-5649165-$ or US-5896521-$ or US-6588006-$ or US-6678873-$).did. or (US-6477683-$ or US-6044211-$).did. or (US-20010034876-$).did.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:31
-	0	((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and ((netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared)) and ((US-6505339-$ or US-6226776-$ or US-6026219-$ or US-5764951-$ or US-6625797-$ or US-6608638-$ or US-6415420-$ or US-6519742-$ or US-6035123-$ or US-5819064-$ or US-5706205-$ or US-5696956-$ or US-5650948-$ or US-6389587-$ or US-6360355-$ or US-6219628-$ or US-5652875-$ or US-5541849-$ or US-6588004-$ or US-6505340-$ or US-6080204-$ or US-5870308-$ or US-5649165-$ or US-5896521-$ or US-6588006-$ or US-6678873-$).did. or (US-6477683-$ or US-6044211-$).did. or (US-20010034876-$).did.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:31
-	1	(optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and ((netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared)) and ((US-6505339-$ or US-6226776-$ or US-6026219-$ or US-5764951-$ or US-6625797-$ or US-6608638-$ or US-6415420-$ or US-6519742-$ or US-6035123-$ or US-5819064-$ or US-5706205-$ or US-5696956-$ or US-5650948-$ or US-6389587-$ or US-6360355-$ or US-6219628-$ or US-5652875-$ or US-5541849-$ or US-6588004-$ or US-6505340-$ or US-6080204-$ or US-5870308-$ or US-5649165-$ or US-5896521-$ or US-6588006-$ or US-6678873-$).did. or (US-6477683-$ or US-6044211-$).did. or (US-20010034876-$).did.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:31
-	35	(((netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))) and (@ad<=20000807 or @rlad<=20000807)) and (VHDL or HDL or Verilog)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:33

-	16	((((netlist or ((hardware or circuit$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))) and (@ad<=20000807 or @rlad<=20000807)) and (VHDL or HDL or Verilog)) and (pipelin$4 or speculat$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 09:41
-	10	(((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807)) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) not ((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and ((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing))))) and Gupta.in.) and "C"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 11:12

-	10	((((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<=20000807 or @rlad<=20000807)) and (optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing)))) not ((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and ((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing)))) and (@ad<=20000807 or @rlad<=20000807)) and (((optimiz$5 and (speculat$5 or (loop near2 pipelin$4) or (block near3 sharing))) and speculat$5 or ((loop near2 pipelin$4) and (block near3 sharing))) and (speculat$5 and (block near3 sharing))))))) and Gupta.in.) and "C"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 11:13
-	414	((bit or flag or wire) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:06
-	5463	(HDL or Verilog or "hardware description language") and (synthesis or netlist)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:00
-	216506	("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:01
-	174	(@ad<=20000807 or @rlad<=20000807) and (emulation or cosimulat$4 or co-simulat$4 or synthesis) and (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((HDL or Verilog or "hardware description language") and (synthesis or netlist)) and compiler	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:02
-	368	(@ad<=20000807 or @rlad<=20000807) and (((bit or flag or wire) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:03

-	174	((@ad<=20000807 or @rlad<=20000807) and (emulation or cosimulat$4 or co-simulat$4 or synthesis) and (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((HDL or Verilog or "hardware description language") and (synthesis or netlist)) and compiler) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:03
-	174	(@ad<=20000807 or @rlad<=20000807) and (((@ad<=20000807 or @rlad<=20000807) and (emulation or cosimulat$4 or co-simulat$4 or synthesis) and (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))) and ((HDL or Verilog or "hardware description language") and (synthesis or netlist)) and compiler) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block)))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:03
-	144	((@ad<=20000807 or @rlad<=20000807) and (((bit or flag or wire) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:06
-	144	(@ad<=20000807 or @rlad<=20000807) and (((@ad<=20000807 or @rlad<=20000807) and (((bit or flag or wire) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block)))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:09
-	1	((@ad<=20000807 or @rlad<=20000807) and (((bit or flag or wire) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) and (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:04

-	51	(((@ad<=20000807 or @rlad<=20000807) and (((bit or flag or wire) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))))) and ((bit near2 (first or last or one)) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:08
-	0	((((@ad<=20000807 or @rlad<=20000807) and (((bit or flag or wire) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))))) and ((bit near2 (first or last or one)) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3))) and (((("flow graph" or (loop adj2 schedul$5)) same "high-level programming") and (optimi$5 and (hardware same (synthesis or netlist))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:09
-	51	(@ad<=20000807 or @rlad<=20000807) and ((((@ad<=20000807 or @rlad<=20000807) and (((bit or flag or wire) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))))) and ((bit near2 (first or last or one)) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:22
-	2	((@ad<=20000807 or @rlad<=20000807) and ((((@ad<=20000807 or @rlad<=20000807) and (((bit or flag or wire) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable) and (synthesis same (hardware or circuit$4)) and CFG or (control adj2 (flow or block))))) and ((bit near2 (first or last or one)) near6 (indicat$4 or represent$3 or defin$4)) near4 (variable near3 (declar$3 or exist$2 or defin$3)))) not (Silverbrook.in.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:19
-	4	(netlist or synthesis and (RTL or HDL)) and (wires near3 ((defin$4 or represent$4) near4 variable))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:21

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-	4	(@ad<=20000807 or @rlad<=20000807) and ((netlist or synthesis and (RTL or HDL)) and (wires near3 ((defin$4 or represent$4) near4 variable)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:29
-	3	((@ad<=20000807 or @rlad<=20000807) and ((netlist or synthesis and (RTL or HDL)) and (wires near3 ((defin$4 or represent$4) near4 variable))) and pars$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 12:30
-	3	(execute near5 (block near6 speculation))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 18:12
-	1	(execut$4 near5 ("in parallel" near6 speculati$5)) and (block same (optimi$6 or basic)) and 717/$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 18:14
-	0	(execut$4 near5 ((parallel$5 or simultane$5) near6 speculati$5)) and (block same (optimi$6 or basic)) and (Schlansker or Gupta).in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 18:15
-	1	(((parallel$5 or simultane$5) near6 speculati$5)) and (block same (optimi$6 or basic)) and (Schlansker or Gupta).in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/06 18:19